REMARKS/ARGUMENTS

Claim 2 was rejected under 35 U.S.C. §112, paragraph 2, on the ground that in the Examiner's opinion, the current mirror was part of the comparator and therefore it was improper to recite the current mirror and the comparator as separate elements in claim 2.

The rejection is respectfully traversed. As shown in Fig. 6, the current mirror circuit comprises two bipolar transistors (not numbered) and two current sources I and NI see Fig. 2 and page 1, lines 15-21). On the other hand, the comparator is made up of FETs Q2, Q3 and Q4 (see page 5, lines 1-10).

Therefore, the current mirror and the comparator are separate elements and can be claimed as such.

Since claim 2 was not rejected over any prior art, allowance of claim 2 is requested.

Claims 1 and 3 were rejected as being anticipated by Fischer. Claim 1 is being canceled, and claim 3 is being amended to recite, in part, a combination of a first bipolar transistor providing V_{be}, two additional bipolar transistors in a current mirror circuit providing ΔV_{be}, a comparator that receives V_{be} and ΔV_{be}, and other features. No such combination is seen in the art. Allowance is therefore requested.

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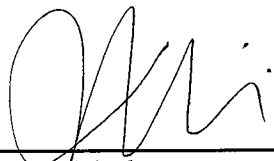
JAF:lf

Respectfully submitted,



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